CLAIM AMENDMENTS

Claim 1 (currently amended) A system comprising:

a first transmitter having a first data input terminal that receives first transmit data, a first transmit clock terminal that receives a first transmit clock of a transmit frequency, and a first data output terminal that transmits the first transmit data synchronized with the first transmit clock;

a second transmitter having a second data input terminal that receives second transmit data, a second transmit clock terminal that receives a second transmit clock of the transmit frequency, and a second data output terminal that transmits the second transmit data synchronized with the second transmit clock; and

a ~~phase adjustment~~ phase-adjustment circuit that derives the first transmit clock and the second transmit clock from a reference clock signal and adjusts the first transmit clock with respect to the second transmit clock to vary the phase of the first transmit data with respect to the second transmit data;

wherein the phase-adjustment circuit dynamically varies the phase of the first transmit data with respect to the second transmit data to misalign the first and second transmit data at a victim receiver.

Claim 2 (canceled)

Claim 3 (previously presented) The system of claim 1, wherein the phase-adjustment circuit includes a phase mixer.

Claim 4 (original) The system of claim 3, wherein the phase-adjustment circuit further includes a phase control circuit coupled to the phase mixer.

Claim 5 (previously presented) The system of claim 1, wherein the phase-adjustment circuit includes a counter that issues periodic select signals to the phase mixer during transmission of at least one of the first and second transmit data.

Claim 6 (previously presented) The system of claim 1, wherein the phase-adjustment circuit includes a phase.mixer, the system further comprising a locked-loop circuit connected to the mixer, and wherein the locked-loop circuit delivers a plurality of reference-clock phase vectors to the phase mixer.

Claim 7 (original) The system of claim 1, further comprising:

a first transmission channel coupled to the first transmitter output terminal, wherein the first transmission channel conveys the first transmitted data;

a second transmission channel coupled to the second transmitter output terminal, wherein the second transmission channel conveys the second transmitted data; and

a receiver having a receiver input node coupled to the first transmitter output terminal via the first transmission channel, wherein the receiver input node receives the first transmitted data, and wherein the receiver input node receives an artifact of the second transmitted data as crosstalk coupled from the second transmission channel to the first transmission channel.

Claim 8 (previously presented) A system comprising:

a transmitter having a data input terminal that receives first transmit data, a transmit clock terminal that receives a transmit clock of a transmit frequency, and a data output terminal that transmits the first transmit data synchronized with the transmit clock;

a first communication channel coupled to the first data output terminal, wherein the first communication channel receives the first transmit data;

a first receiver having a first receiver input node coupled to the first data output terminal via the first communication channel, wherein the first receiver input node receives the first transmitted data from the transmitter;

a second communication channel that conveys second transmit data;

a second receiver having a second receiver input node coupled to the second communication channel, wherein the second receiver input node receives the second transmit data and crosstalk artifacts of the first transmitted data; and

a phase adjustment circuit connected to the transmit clock terminal of the transmitter, wherein the phase adjustment circuit adjusts the first transmit clock to vary the timing of the crosstalk artifacts with respect to the second transmit data;

wherein the phase adjustment circuit dynamically varies the timing of the first transmit data with respect to the second transmit data.

Claim 9 (original) The system of claim 8, wherein the second communication channel conveys the second transmit data at the transmit frequency.

Claim 10 (canceled)

Claim 11 (currently amended) The system of claim [[10]] 8, wherein the phase-adjustment circuit includes a phase mixer.

Claim 12 (currently amended) The system of claim [[10]] 8, wherein the phase-adjustment circuit further includes a phase control circuit connected to the phase mixer.

Claim 13 (original) The system of claim 12, wherein the phase-adjustment circuit includes a counter that issues periodic select signals to the phase mixer during transmission of at least one of the first and second transmit data.

Claim 14 (currently amended) The system of claim [[10]] 8, wherein the phase-adjustment circuit includes a phase mixer, the system further comprising a loop circuit connected to the mixer, and wherein the loop circuit delivers to the phase mixer a plurality of reference-clock phase vectors.

Claim 15 (original) The system of claim 8, wherein the loop circuit comprises a phase-locked loop.

Claim 16 (currently amended) A transceiver comprising:

a reference clock source that produces a reference clock;

a loop circuit coupled to the reference clock source, wherein the loop circuit derives a plurality of clocks of different clock phases from the reference clock;

a first transmit mixer coupled to the loop circuit, wherein the first transmit mixer derives a first transmit clock from the clocks of different clock phases, the first transmit mixer including a first phase control port;

a first transmit phase controller coupled to the first phase control port, wherein the first transmit phase controller issues first transmit-phase control signals via the first phase control port to alter the phase of the first transmit clock; [[and]]

a first transmitter that transmits first data ~~samples~~ synchronized with the first transmit clock;

a second transmit mixer coupled to the loop circuit, wherein the second transmit mixer derives a second transmit clock from the clocks of different clock phases, the second transmit mixer including a second phase control port;

a second transmit phase controller coupled to the second phase control port, wherein the second transmit phase controller issues second transmit-phase control signals via the second phase control port to alter the phase of the second transmit clock; and

a second transmitter that transmits second data synchronized with the second transmit clock;

wherein at least one of the first and second transmit phase controllers dynamically control the respective first and second phase control signals to misalign the first and second data.

Claim 17 (currently amended) The transceiver of claim 16, wherein the first and second transmitters are instantiated on a first integrate circuit, and ~~transmitter phase controller issues a plurality of the transmit-phase control signals as the transmitter transmits the data samples~~ the at least one of the first and second transmit phase controllers dynamically varies the phase of the first data with respect to the second data to misalign the first and second data at a victim receiver instantiated on a second integrated circuit.

Claim 18 (currently amended) The transceiver of claim 16, further comprising:

a receive mixer coupled to the loop circuit, wherein the receive mixer derives a receive clock from the clocks of different phases;

a receive phase controller coupled to the second phase control port, wherein the receive phase controller issues receive-phase control signals via the second phase control port to alter the phase of the receive clock; and

a receiver that receives data samples synchronized with the receive clock;

wherein the at least one of the first and second transmit phase controllers dynamically varies the phase of the first data with respect to the second data to misalign the first and second data at a the receiver.

Claim 19 (currently amended) The transceiver of claim 16, further comprising a resynchronizer that produces the first ~~transmit~~ data synchronized with the first transmit clock from transmit data synchronized with a ~~second~~ third clock.

Claim 20 (currently amended) The transceiver of claim 19, further comprising a serializer disposed between the resynchronizer and the first transmitter.

Claim 21 (original) A method comprising:

transmitting first and second data signals timed to respective first and second transmit clocks to respective first and second receivers;

monitoring an output of the second receiver for errors induced by the first data signal; and

adjusting, in response to the monitoring, the timing of the first transmit clock in relation to the second transmit clock.

Claim 22 (original) The method of claim 21, wherein the monitoring includes calculating the bit-error rate of the second receiver.

Claim 23 (original) The method of claim 22, wherein the adjusting reduces the bit-error rate.

Claim 24 (original) The method of claim 21, further comprising dynamically adjusting the timing of the first transmit clock relative to the second transmit clock while transmitting the first and second data signals.

Claim 25 (original) A method comprising:

transmitting first, second, and third data signals timed to respective first and second transmit clocks to respective first and second receivers over respective first and second communication channels, wherein the first data signal induces crosstalk artifacts in the second communication channel; and

adjusting the phase of the first transmit clock in relation to the second transmit clock while transmitting the first and second data signals.

Claim 26 (currently amended) A system comprising:

a first transmitter having a first data input terminal that receives first transmit data, a first transmit clock terminal that receives a first transmit clock of a transmit frequency, and a first data output terminal that transmits the first transmit data synchronized with the first transmit clock;

a second transmitter having a second data input terminal that receives second transmit data, a second transmit clock terminal that receives a second transmit clock of the transmit frequency, and a second data output terminal that transmits the second transmit data synchronized with the second transmit clock; and

dynamic phase-adjusting means for periodically or continuously adjusting the first transmit clock to vary the timing of the first transmit data with respect to the second transmit data to misalign the first and second transmit data at a victim receiver.

Claim 27 (original) The system of claim 26, wherein the phase-adjusting means dynamically varies the timing of the first transmit data with respect to the second transmit data.

Claim 28 (original) The system of claim 27, wherein the phase-adjusting means issues

periodic select signals to the phase mixer during transmission of at least one of the first and second transmit data.

Claim 29 (previously presented) A communication system comprising:

a. a first transmitter driven by a first transmit clock signal of a first phase, the first transmitter adapted to transmit first data synchronized to the first transmit clock signal;

b. a first communication channel coupled to the first transmitter and conveying the first transmit data;

c. at least one aggressor transmitter driven by a second transmit clock signal of an aggressor data phase, the aggressor transmitter adapted to transmit second data synchronized to the second transmit clock signal;

d. a second communication channel coupled to the second transmitter and conveying the second transmit data; and

e. a victim receiver coupled to the first communication channel and adapted to sample the first transmit data using a receive clock signal of a victim data phase, the victim receiver additionally receiving cross-talk artifacts of the second transmit data;

f. wherein at least one of the aggressor transmitter and the victim receiver includes phase-adjustment circuitry adapted to dynamically alter the aggressor data phase relative to the victim data phase to reduce crosstalk from the aggressor transmitter to the victim receiver.

Claim 30 (original) The communication system of claim 29, wherein the crosstalk is FEXT.

Claim 31 (original) The communication system of claim 30, wherein the crosstalk is NEXT.

Claim 32 (previously presented) The system of claim 1, further comprising: a receiver coupled to the second transmitter to receive the second transmit data and to produce an error signal in response to the second transmit data; and a system phase

controller coupled to the receiver and to the phase adjustment circuit, wherein the system phase controller issues a control signal to the phase adjustment circuit.

Claim 33 (previously presented) The system of claim 32, wherein the first transmitter induces FEXT at the receiver.

Claim 34 (previously presented) The system of claim 32, wherein the first transmitter induces NEXT at the receiver.

Claim 35 (previously presented) The system of claim 1, wherein the first transmit data includes leading and trailing edges, and wherein the phase adjustment circuit independently adjusts the timing of the leading and trailing edges.